Features

- Utilizes the ARM7TDMI® ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - Embedded ICE (In Circuit Emulation)
- 3K Bytes Internal RAM
- Fully Programmable External Bus Interface (EBI)
  - Maximum External Address Space of 64M Bytes
  - Up to Eight Chip Selects
  - Software Programmable 8/16-bit External Data Bus
- 8-channel Peripheral Data Controller
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - Five External Interrupts, including a High-priority, Low-latency Interrupt Request
- 58 Programmable I/O Lines
- 6-channel 16-bit Timer/Counter
  - Six External Clock Inputs
  - Two Multi-purpose I/O Pins per Channel
- 3 USARTs
  - Two Dedicated Peripheral Data Controller (PDC) Channels per USART
  - Support for up to 9-bit Data Transfers
- Master/Slave SPI Interface
  - Two Dedicated Peripheral Data Controller (PDC) Channels
  - 8- to 16-bit Programmable Data Length
  - 4 External Slave Chip Selects
- Programmable Watchdog Timer
- Power Management Controller (PMC)
  - CPU and Peripherals can be Deactivated Individually
- IEEE 1149.1 JTAG Boundary Scan on all Active Pins
- Fully Static Operation: 0 Hz to 25 MHz (12 MHz @ 1.8V)
- 1.8V to 3.6V Core Operating Voltage Range
- 2.7V to 5.5V I/O Operating Voltage Range
- -40° to +85° C Operating Temperature Range
- Available in a 144-ball PBGA Package

AT91 ARM® Thumb® Microcontrollers

AT91M43300

1322B–ATARM–12-Dec-05

1. Description

The AT91M43300 is a member of the Atmel AT91 16/32-bit Microcontroller family which is based on the ARM7TDMI processor core.

This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and features very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The AT91 ARM-based MCU family also features Atmel's high-density, in-system programmable, nonvolatile memory technology.

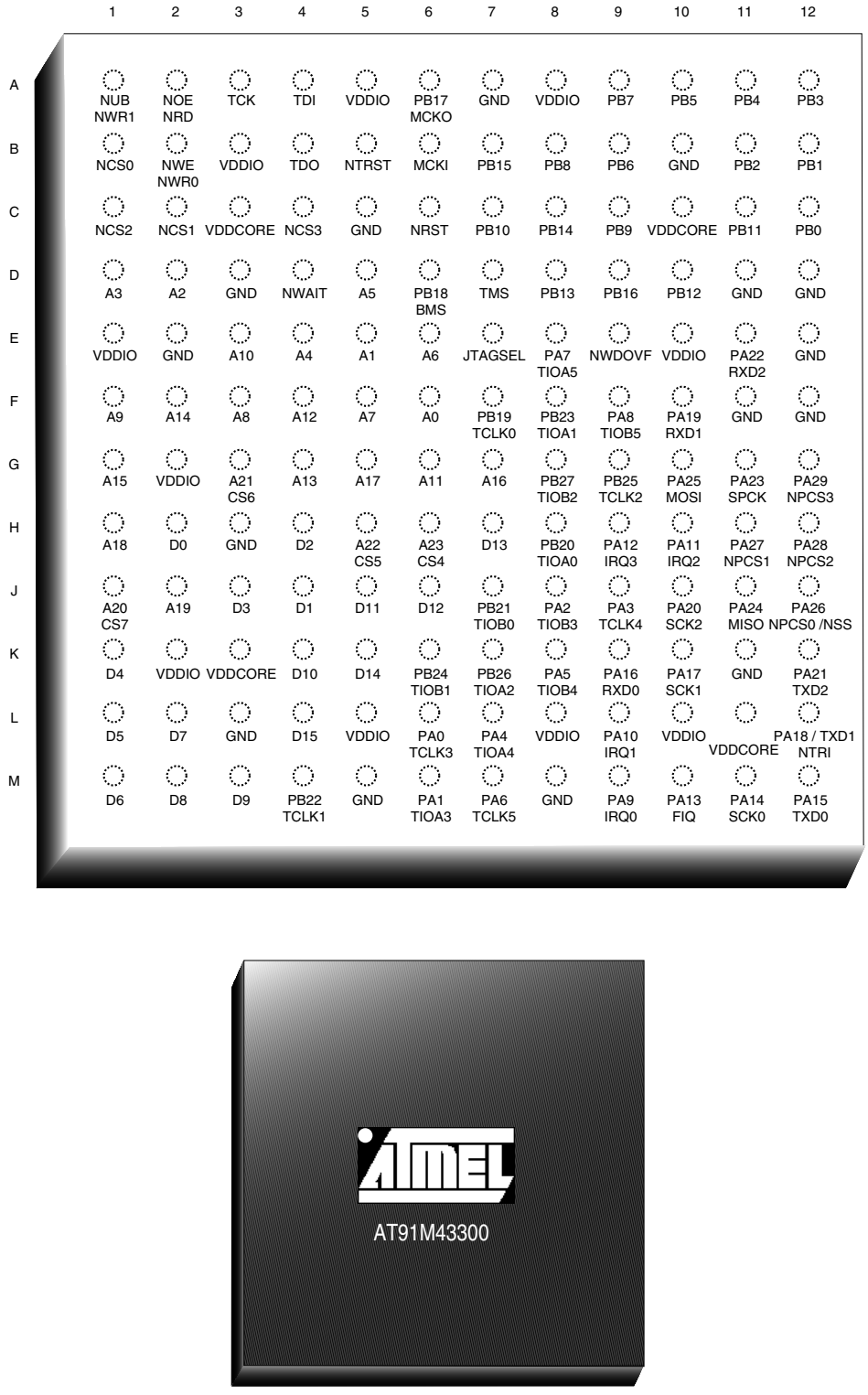
The AT91M43300 has a direct connection to off-chip memory, including Flash, through the fully programmable External Bus Interface.

The AT91M43300 is manufactured using Atmel's high density CMOS technology. By combining the ARM7TDMI microcontroller core with an on-chip SRAM, and a wide range of peripheral functions on a monolithic chip, the AT91M43300 provides a highly flexible and cost-effective solution to many compute-intensive multi-processor applications.

The compact BGA package reduces required board space to an absolute minimum.

2. Pin Configuration

Figure 2-1. AT91M43300 in BGA144 Package (top view)



3. Pin Description

Table 3-1. AT91M43300 Pin Description

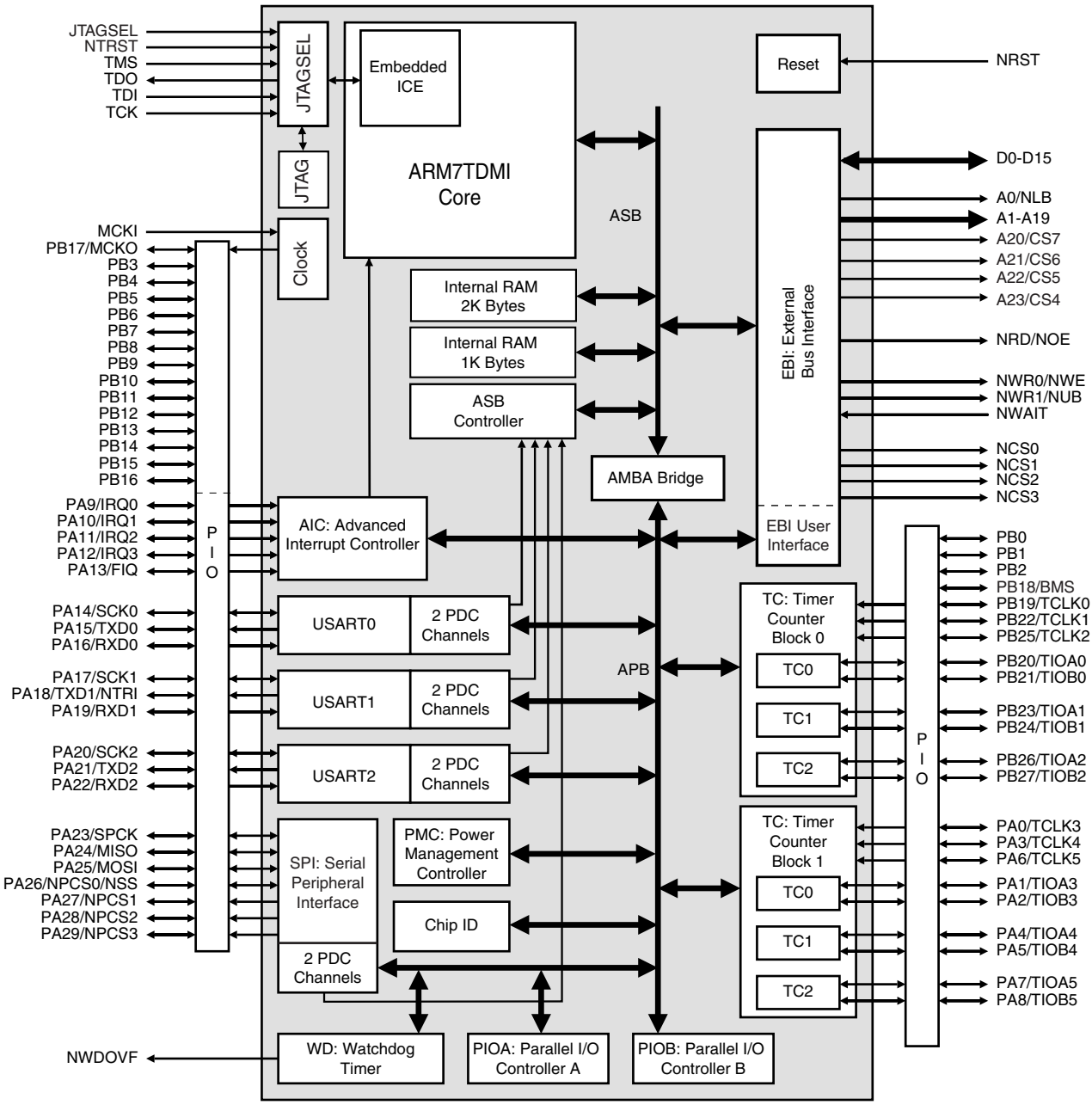
Module	Name	Function	Type	Active	Comments
EBI	A0 - A23	Address Bus	Output	–	All valid after reset
	D0 - D15	Data Bus	I/O	–	
	CS4 - CS7	Chip Select	Output	High	A23 - A20 after reset
	NCS0 - NCS3	Chip Select	Output	Low	
	NWR0	Lower Byte 0 Write Signal	Output	Low	Used in Byte Write option
	NWR1	Lower Byte 1 Write Signal	Output	Low	Used in Byte Write option
	NRD	Read Signal	Output	Low	Used in Byte Write option
	NWE	Write Enable	Output	Low	Used in Byte Select option
	NOE	Output Enable	Output	Low	Used in Byte Select option
	NUB	Upper Byte Select (16-bit SRAM)	Output	Low	Used in Byte Select option
	NLB	Lower Byte Select (16-bit SRAM)	Output	Low	Used in Byte Select option
	NWAIT	Wait Input	Input	Low	
	BMS	Boot Mode Select	Input	–	Sampled during reset
AIC	IRQ0 - IRQ3	External Interrupt Request	Input	–	PIO-controlled after reset
	FIQ	Fast External Interrupt Request	Input	–	PIO-controlled after reset
Timer	TCLK0 - TCLK5	Timer External Clock	Input	–	PIO-controlled after reset
	TIOA0 - TIOA5	Multipurpose Timer I/O Pin A	I/O	–	PIO-controlled after reset
	TIOB0 - TIOB5	Multipurpose Timer I/O Pin B	I/O	–	PIO-controlled after reset
USART	SCK0 - SCK2	External Serial Clock	I/O	–	PIO-controlled after reset
	TXD0 - TXD2	Transmit Data Output	Output	–	PIO-controlled after reset
	RXD0 - RXD2	Receive Data Input	Input	–	PIO-controlled after reset
SPI	SPCK	SPI Clock	I/O	–	PIO-controlled after reset
	MISO	Master In Slave Out	I/O	–	PIO-controlled after reset
	MOSI	Master Out Slave In	I/O	–	PIO-controlled after reset
	NSS	Slave Select	Input	Low	PIO-controlled after reset
	NPCS0 - NPCS3	Peripheral Chip Select	Output	Low	PIO-controlled after reset
PIO	PA0 - PA29	Programmable I/O Port A	I/O	–	Input after reset
	PB0 - PB27	Programmable I/O Port B	I/O	–	Input after reset
WD	NWDOVF	Watchdog Timer Overflow	Output	Low	Open drain
Clock	MCKI	Master Clock Input	Input	–	Schmidt trigger
	MCKO	Master Clock Output	Output	–	
Reset	NRST	Hardware Reset Input	Input	Low	Schmidt trigger, internal pull-up

Table 3-1. AT91M43300 Pin Description (Continued)

Module	Name	Function	Type	Active	Comments
JTAG/ICE	JTAGSEL	Selects between JTAG and ICE mode	Input		High enables IEEE 1149.1 JTAG boundary scan
	TMS	Test Mode Select	Input	–	Schmidt trigger, internal pull-up
	TDI	Test Data In	Input	–	Schmidt trigger, internal pull-up
	TDO	Test Data Out	Output	–	
	TCK	Test Clock	Input	–	Schmidt trigger, internal pull-up
	NTRST	Test Reset Input	Input	Low	Schmidt trigger, internal pull-up
Power	VDDIO	I/O Power	Power	–	3V or 5V nominal supply
	VDDCORE	Core Power	Power	–	2.0V or 3V nominal supply
	GND	Ground	Ground	–	
Emulation	NTRI	Tristate Mode Enable	Input	Low	Sampled during reset

4. Block Diagram

Figure 4-1. AT91M43300



5. Architectural Overview

The AT91M43300 architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories and the external memories and devices by means of the External Bus Interface (EBI). The APB is designed for accesses to on-chip peripherals and is optimized for low power consumption. The AMBA Bridge provides an interface between the ASB and the APB.

An on-chip Peripheral Data Controller (PDC) transfers data between the on-chip USARTs/SPI and the on and off-chip memories without processor intervention. Most importantly, the PDC removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64k contiguous bytes without reprogramming the starting address. As a result, the performance of the microcontroller is increased and the power consumption reduced.

The AT91M43300 peripherals are designed to be easily programmable with a minimum number of instructions. Each peripheral has a 16K byte address space allocated in the upper 3M bytes of the 4G byte address space. Except for the interrupt controller, the peripheral base address is the lowest address of its memory space. The peripheral register set is composed of control, mode, data, status and interrupt registers.

To maximize the efficiency of bit manipulation, frequently written registers are mapped into three memory locations. The first address is used to set the individual register bits, the second resets the bits and the third address reads the value stored in the register. A bit can be set or reset by writing a one to the corresponding position at the appropriate address. Writing a zero has no effect. Individual bits can thus be modified without having to use costly read-modify-write and complex bit manipulation instructions.

All of the external signals of the on-chip peripherals are under the control of the Parallel I/O controller. The PIO controller can be programmed to insert an input filter on each pin or generate an interrupt on a signal change. After reset, the user must carefully program the PIO Controller in order to define which peripheral signals are connected with off-chip logic.

The ARM7TDMI processor operates in little-endian mode in the AT91M43300 microcontroller. The processor's internal architecture and the ARM and Thumb instruction sets are described in the ARM7TDMI Datasheet. The memory map and the on-chip peripherals are described in the datasheet entitled "AT91M63200 Datasheet" (Literature No. 1028). Electrical characteristics for the AT91M43300 are documented in the "AT91M63200 Electrical and Mechanical Characteristics" (Literature No. 1090).

The ARM Standard In-Circuit-Emulation debug interface is supported via the ICE port of the AT91M43300 via the JTAG/ICE port when JTAGSEL is low. IEEE JTAG boundary scan is supported via the JTAG/ICE port when JTAGSEL is high.

5.1 PDC: Peripheral Data Controller

The AT91M43300 has an 8-channel PDC dedicated to the three on-chip USARTs and to the SPI. One PDC channel is connected to the receiving channel and one to the transmitting channel of each peripheral.

The user interface of a PDC channel is integrated in the memory space of each USART channel and in the memory space of the SPI. It contains a 32-bit address pointer register and a 16-bit count register. When the programmed data is transferred, an end of transfer interrupt is gener-

ated by the corresponding peripheral. See the USART section and the SPI section for more details on PDC operation and programming.

5.2 Power Supplies

The AT91M43300 has two kinds of power supply pins:
- VDDCORE pins, which power the chip core
- VDDIO pins, which power the I/O lines

This allows core power consumption to be reduced by supplying it with a lower voltage than the I/O lines. The VDDCORE pins must never be powered at a voltage greater than the supply voltage applied to the VDDIO pins.

Typical supported voltage combinations are shown in the following table:

Pins	Typical Supply Voltages		
VDDCORE	3.0V or 3.3V	3.0V or 3.3V	2.0V
VDDIO	5.0V	3.0V or 3.3V	3.0V or 3.3V

6. EBI: External Bus Interface

The EBI generates the signals which control the access to the external memory or peripheral devices. The EBI is fully programmable and can address up to 64M bytes. It has eight chip selects and a 24-bit address bus, the upper four bits of which are multiplexed with a chip select.

The 16-bit data bus can be configured to interface with 8- or 16-bit external devices. Separate read and write control signals allow for direct memory and peripheral interfacing.

The EBI supports different access protocols allowing single clock cycle memory accesses.

The main features are:
- External memory mapping
- Up to 8 chip select lines
- 8- or 16-bit data bus
- Byte write or byte select lines
- Remap of boot memory
- Two different read protocols
- Programmable wait state generation
- External wait request
- Programmable data float time

7. AIC: Advanced Interrupt Controller

The AT91M43300 has an 8-level priority, individually maskable, vectored interrupt controller. This feature substantially reduces the software and real time overhead in handling internal and external interrupts.

The interrupt controller is connected to the NFIQ (fast interrupt request) and the NIRQ (standard interrupt request) inputs of the ARM7TDMI processor. The processor's NFIQ line can only be asserted by the external fast interrupt request input: FIQ. The NIRQ line can be asserted by the interrupts generated by the on-chip peripherals and the external interrupt request lines: IRQ0 to IRQ3.

An 8-level priority encoder allows the customer to define the priority between the different NIRQ interrupt sources.

Internal sources are programmed to be level sensitive or edge triggered. External sources can be programmed to be positive or negative edge triggered or high or low level sensitive.

8. PIO: Parallel I/O Controller

The AT91M43300 features 58 programmable I/O lines. 14 pins on the AT91M43300 are dedicated as general purpose I/O pins. Other I/O lines are multiplexed with on-chip peripheral I/O signals in order to optimize the use of available package pins. The I/O lines are controlled by two separate and identical PIO Controllers (PIOA and PIOB). Each PIO controller also provides an internal interrupt signal to the Advanced Interrupt Controller (AIC).

9. USART: Universal Synchronous/Asynchronous Receiver/Transmitter

The AT91M43300 provides three identical, full-duplex, universal synchronous/asynchronous receiver/transmitters that interface to the APB and are connected to the Peripheral Data Controller.

The main features are:
- Programmable Baud Rate Generator
- Parity, Framing and Overrun Error Detection
- Line Break Generation and Detection
- Automatic Echo, Local Loopback and Remote Loopback channel modes
- Multi-drop Mode: Address Detection and Generation
- Interrupt Generation
- Two Dedicated Peripheral Data Controller channels
- 5-, 6-, 7-, 8- and 9-bit character length

10. SPI: Serial Peripheral Interface

The AT91M43300 features an SPI which provides communication with external devices in master or slave mode.

The SPI has four external chip selects which can be connected to up to 15 devices. The data length is programmable, from 8 to 16-bit.

As for the USART, a 2-channel PDC is used to move data directly between memory and the SPI without CPU intervention for maximum real-time processing throughput.

11. TC: Timer Counter

The AT91M43300 features two identical Timer Counter blocks, each containing three identical 16-bit timer counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

Each Timer Counter channel has 3 external clock inputs, 5 internal clock inputs, and 2 multi-purpose input/output signals which can be configured by the user. Each channel drives an internal interrupt signal which can be programmed to generate processor interrupts via the Advanced Interrupt Controller (AIC).

Each Timer Counter block features two global registers which act upon all three TC channels. The Block Control Register allows the three channels to be started simultaneously with the same instruction. The Block Mode Register defines the external clock inputs for each Timer Counter channel, allowing them to be chained.

12. WD: Watchdog Timer

The AT91M43300 features an internal Watchdog Timer which can be used to guard against system lock-up if the software becomes trapped in a deadlock.

13. PMC: Power Management Controller

The Power Management Controller allows optimization of power consumption. The PMC enables/disables the clock inputs to most of the peripherals as well as to the ARM processor core.

When the ARM core clock is disabled, the current instruction is processed before the clock is stopped. The clock can be re-enabled by any enabled interrupt or by a hardware reset.

When a peripheral clock is disabled, the clock is immediately stopped. When the clock is re-enabled, the peripheral resumes action where it left off.

Due to the static nature of the design, the contents of the on-chip RAM and registers for which the clocks are disabled remain unchanged

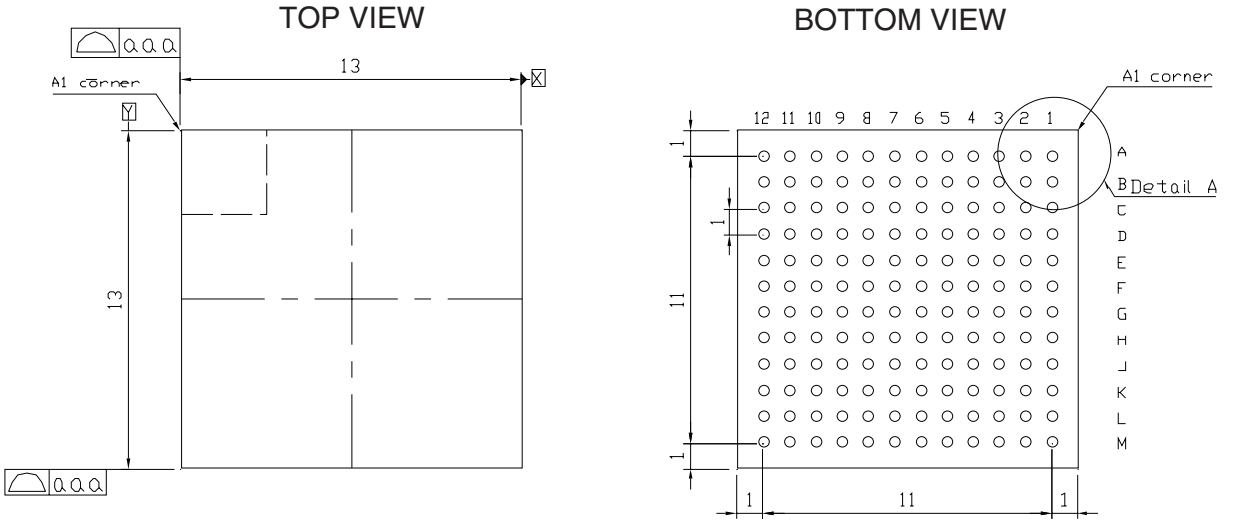
14. SF: Special Function

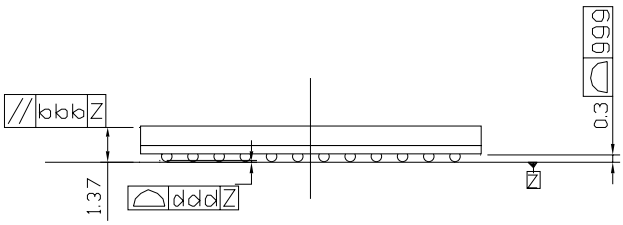
The AT91M43300 provides registers which implement the following special functions.

- Chip identification
- RESET status

15. Package Outline BGA144

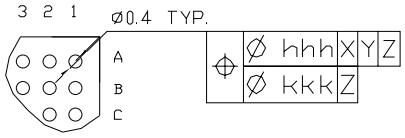
Figure 15-1. 144-ball Ball Grid Array Package





SIDE VIEW

Symbol	Max.
aaa	0.1
bbb	0.3
ddd	0.15
ggg	0.03
hhh	0.1
kkk	0.1



Detail A

NOTES

1. Package dimensions conform to JESD-95-1 Section 5
2. Dimensioning and tolerancing per ASME Y14.5M-1994
3. All dimensions in mm
4. Solder Ball position designation per JESD 95-1, SPP-010
5. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls

16. Soldering Profile

16.1 Standard Soldering Profile

Table 16-1 gives the recommended soldering profile from J-STD-20.

Table 16-1. Soldering Profile

	Convection or IR/Convection	VPR
Average Ramp-up Rate (183° C to Peak)	3° C/sec. max.	10° C/sec.
Preheat Temperature 125° C ±25° C	120 sec. max	
Temperature Maintained Above 183° C	60 sec. to 150 sec.	
Time within 5° C of Actual Peak Temperature	10 sec. to 20 sec.	60 sec.
Peak Temperature Range	220 +5/-0° C or 235 +5/-0° C	215 to 219° C or 235 +5/-0° C
Ramp-down Rate	6° C/sec.	10° C/sec.
Time 25° C to Peak Temperature	6 min. max	

Small packages may be subject to higher temperatures if they are reflowed in boards with larger components. In this case, small packages may have to withstand temperatures of up to 235° C, not 220° C (IR reflow).

Recommended package reflow conditions depend on package thickness and volume. See Table 16-2.

Table 16-2. Recommended Package Reflow Conditions (1), (2) (3)

Parameter	Temperature
Convection	220 +5/-0° C
VPR	215 to 219° C
IR/Convection	220 +5/-0° C

Notes:
1. The packages are qualified by Atmel by using IR reflow conditions, not convection or VPR.
2. By default, the package level 1 is qualified at 220° C (unless 235° C is stipulated).
3. The body temperature is the most important parameter but other profile parameters such as total exposure time to hot temperature or heating rate may also influence component reliability.

A maximum of three reflow passes is allowed per component.

16.2 RoHS Soldering Profile

Table 16-3 gives the recommended soldering profile from J-STD-20C.

Table 16-3. Soldering Profile RoHS Compliant Package

Profile Feature	Convection or IR/Convection
Average Ramp-up Rate (183° C to Peak)	3° C/sec. max.
Preheat Temperature 125° C ±25° C	180 sec. max
Temperature Maintained Above 183° C	60 sec. to 150 sec.
Time within 5° C of Actual Peak Temperature	20 sec. to 40 sec.
Peak Temperature Range	260° C
Ramp-down Rate	6° C/sec.
Time 25° C to Peak Temperature	8 min. max

Note: It is recomended to apply a soldering temperature higher than 250°C.

A maximum of three reflow passes is allowed per component.

17. Ordering Information

Table 17-1. Ordering Information

Ordering Code	Package	Package Type	Operating Temperature Range
AT91M43300-25CI	BGA 144	Standard	Industrial (-40° C to 85° C)
AT91M43300-25CJ	BGA 144	RoHS-compliant	

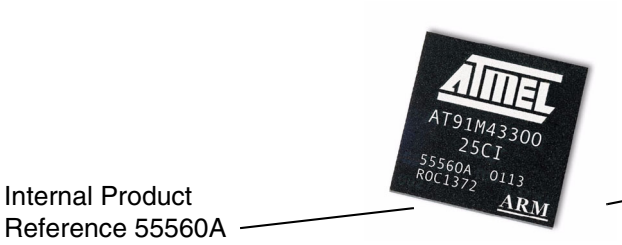
18. AT91M43300 Errata

These errata are applicable to:

AT91M43300 Lit° 1322

AT91M43300,Electrical Characteristics, Rev. 1090B–05/00

- 144-ball BGA devices with the following markings:



18.1 Warning: Additional NWAIT Constraints

When the NWAIT signal is asserted during an external memory access, the following EBI behavior is correct:

- NWAIT is asserted before the first rising edge of the master clock and respects the NWAIT to MCKI rising setup timing as defined in the Electrical Characteristics datasheet.
- NWAIT is sampled inactive and at least one standard wait state remains to be executed, even if NWAIT does not meet the NWAIT to first MCKI rising setup timing (i.e., NWAIT is asserted only on the second rising edge of MCKI).

In these cases, the access is delayed as required by NWAIT and the access operations are correctly performed.

In other cases, the following erroneous behavior occurs:

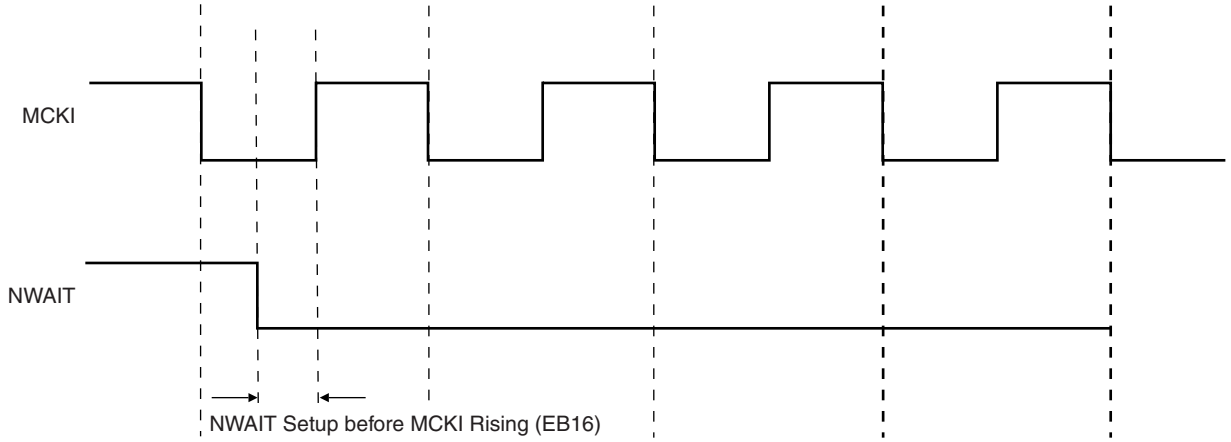
- 32-bit read accesses are not managed correctly and the first 16-bit data sampling takes into account only the standard wait states. 16- and 8-bit accesses are not affected.
- During write accesses of any type, the NWE rises on the rising edge of the last cycle as defined by the programmed number of wait states. However, NWAIT assertion does affect the length of the total access. Only the NWE pulse length is inaccurate.

At maximum speed, asserting the NWAIT in the first access cycle is not possible, as the sum of the timings “MCKI Falling to Chip Select” and “NWAIT setup to MCKI rising” are generally higher than one half of a clock period. This leads to using at least one standard wait state. However, this is not sufficient except to perform byte or half-word read accesses. Word and write accesses require at least two standard wait states.

The following waveforms further explain the issue:

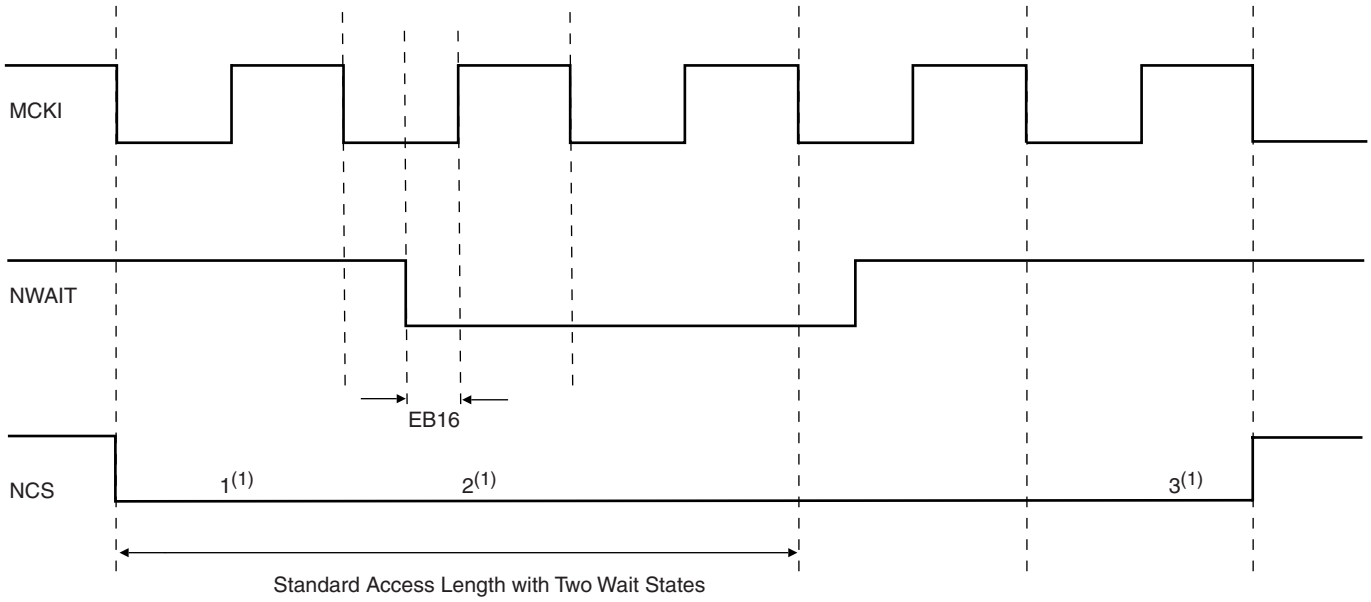
If the NWAIT setup time is satisfied on the first rising edge of MCKI, the behavior is accurate. The EBI operations are not affected when the NWAIT rises.

Figure 18-1. NWAIT Rising



If the NWAIT setup time is satisfied on the following edges of MCKI and if at least one standard wait state remains to be executed, the behavior is accurate. In the following example, the number of standard wait states is two. The NWAIT setup time on the second rising edge of MCKI must be met.

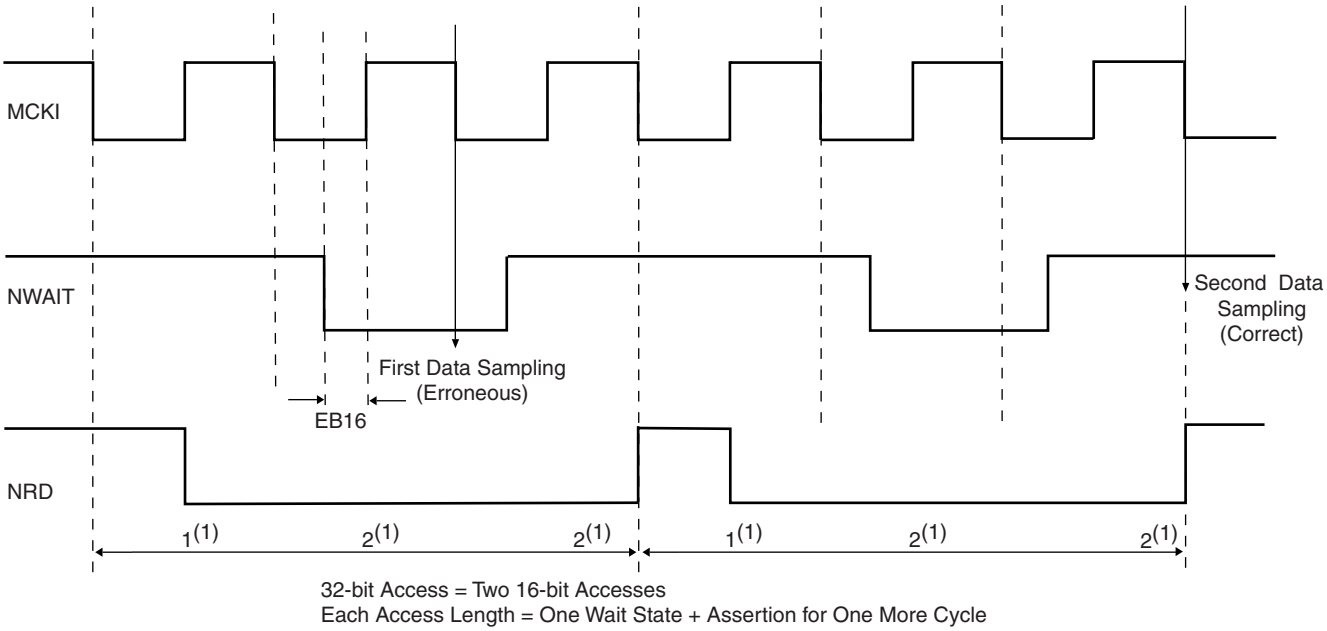
Figure 18-2. Number of Standard Wait States is Two



Note: 1. These numbers refer to the standard access cycles.

If the first two conditions are not met during a 32-bit read access, the first 16-bit data is read at the end of the standard 16-bit read access. In the following example, the number of standard waits is one. NWAIT assertions do affect both NRD pulse lengths, but first data sampling is not delayed. The second data sampling is correct.

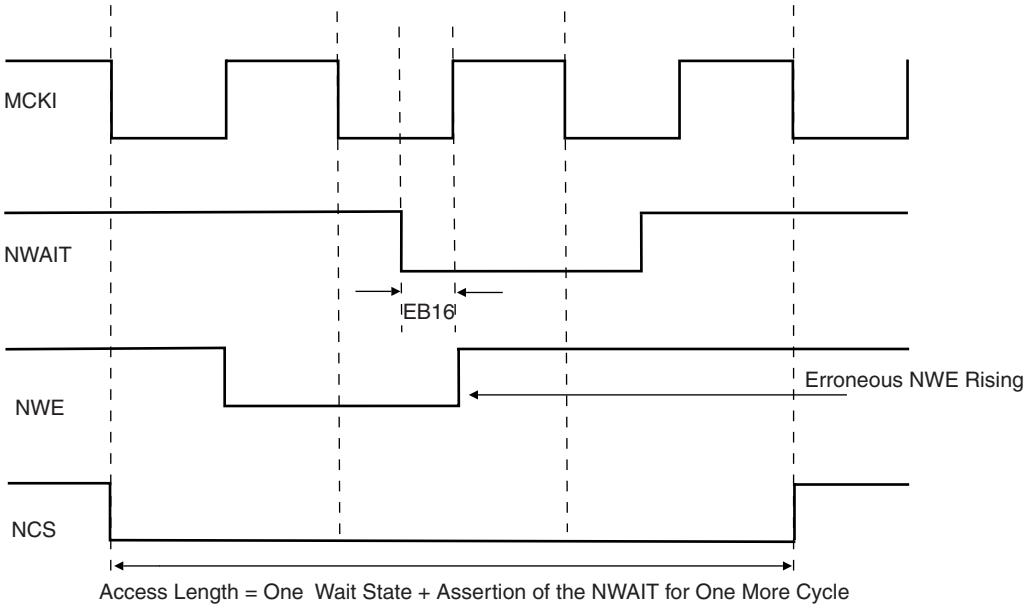
Figure 18-3. Number of Standard Wait States is One



Note: 1. These numbers refer to the standard access cycles.

If the first two conditions are not met during write accesses, the NWE signal is not affected by the NWAIT assertion. The following example illustrates the number of standard wait states. NWAIT is not asserted during the first cycle, but is asserted at the second and last cycle of the standard access. The access is correctly delayed as the NCS line rises accordingly to the NWAIT assertion. However, the NWE signal waveform is unchanged, and rises too early.

Figure 18-4. Description of the Number of Standard Wait States



18.2 Initializing SPI in Master Mode May Cause Problems

Initializing SPI in Master Mode May Cause a Mode Fault Detection

Problem Fix/Workaround

PA26/NPCS0/NSS pin must be pulled up to the V_{DDIO} power supply.

PA26/NPCS0/NSS must be defined as a peripheral pin before programming the SPI peripheral.

18.3 SPI in Slave Mode Does not Work

In transmission, the data to be transmitted (written in SP_TDR) is transferred into the shift register and, consequently, the TDRE bit in SP_SR is set to 1. Though the transfer has not begun, when the following data is written in SP_TDR, it is also transferred into the shift register, crushing the preceding data and setting the bit TDRE to 1.

Problem Fix/Workaround

No work around available.

18.4 Parity Error Bit (PARE) is Set Too Early

The Parity Error bit on the USART is set as soon as the parity bit is detected. However, the faulty character reception status (RXRDY) is set afterwards, only when the stop bit is detected. This is particularly unfortunate when working in Multi-drop mode, as the PARE bit identifies the Address Bytes. When it is detected, the corresponding character has not yet been transferred in the US_RHR register and, therefore, is not yet available.

Problem Fix/Workaround

No problem fix/work around to propose.

19. Revision History

Doc. Rev	Date	Comments	Change Request Ref.
1322A	Sep-09	First issue	
1322B	12-Dec-05	Added Section 16. ”Soldering Profile”, on page 12, Update to Section 17. ”Ordering Information”, on page 14.	1546
		Added Section 18. ”AT91M43300 Errata”, on page 15 Reformat into template version 5.2	

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

1322B–ATARM–12-Dec-05